<u>AMENDMENTS</u>

In the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

- 1. (Currently Amended) A compound semiconductor switching device comprising:
- a first FET comprising signal electrodes and a gate electrode formed on a surface of a channel layer of said first FET, the signal electrodes of the first FET not being connected to each other;

a second FET comprising signal electrodes and a gate electrode formed on a surface of a channel layer of said second FET, the signal electrodes of the second FET not being connected to each other;

a common input terminal, said common input terminal being formed by connecting one of the signal electrodes of the first FET and one of the signal electrodes of the second FET;

a first output terminal, said first output terminal being the signal electrode of the first FET not used as the common input terminal; and

a second output terminal, said second output terminal being the signal electrode of the second FET not used as the common input terminal;

wherein the gate electrodes of the first and second FET's are provided with control signals such that only one FET allows conduction of electric current so that a signal pass is formed between the common input terminal and either the first output terminal or the second output terminal; and

wherein the first FET and the second FET have gate widths of about 700 μ m or less and are not connected to a shunt FET.

- 2. (Original) A compound semiconductor switching device according to claim 1, wherein an input signal of about 2.4 GHz or higher is applied to the common input terminal, and the first FET and the second FET have gate widths of about 600 μ m or less.
- 3. (Currently Amended) A compound semiconductor switching device according to claim 1, further comprising a GaAs substrate [[is]] used as a semi-insulating substrate for forming the channel layer on a surface thereof.
- 4. (Currently Amended) A compound semiconductor switching device according to claim 1, wherein the gate electrode electrodes and the channel layer layers of the first FET and the second FET form respective Schottky contacts, and wherein the signal electrodes and the channel layer layers of the first FET and the second FET form respective ohmic contacts.
- 5. (Original) A compound semiconductor switching device according to claim 1, wherein the signal electrodes of the first FET are a source electrode and a drain electrode of the first FET, and the signal electrodes of the second FET are a source electrode and a drain electrode of the second FET.
- 6. (Original) A compound semiconductor switching device according to claim 1, wherein an input signal of about 2.4 GHz or higher is applied to the common input terminal, and the gates widths of the first FET and the second FET are about 600 μ m or less;

wherein a GaAs substrate is used as a semi-insulating substrate for forming the channel layer on a surface thereof; and

wherein the signal electrodes of the first FET are a source electrode and a drain electrode of the first FET, and the signal electrodes of the second FET are a source electrode and a drain electrode of the second FET.

7. (Currently Amended) A mobile communication device, comprising:

an antenna for receiving and sending an electromagnetic signal;

a signal receiving circuit for receiving the signal through the antenna;

a signal transmitting circuit for sending the signal through the antenna; and

at least one compound semiconductor switching device, said compound semiconductor switching devices comprising:

a first FET comprising signal electrodes and a gate electrode formed on a surface of a channel layer of said first FET, the signal electrodes of the first FET not being connected to each other;

a second FET comprising signal electrodes and a gate electrode formed on a surface of a channel layer of said second FET, the signal electrodes of the second FET not being connected to each other;

a common input terminal, said common input terminal being formed by connecting one of the signal electrodes of the first FET and one of the signal electrodes of the second FET;

a first output terminal, said first output terminal being the signal electrode of the first FET not used as the common input terminal; and

a second output terminal, said second output terminal being the signal electrode of the second FET not used as the common input terminal;

the gate electrodes of the first and second FET's being provided with control signals such that only one FET allows conduction of electric current so that a signal pass is formed between the common input terminal and either the first output terminal or the second output terminal; and

Best Available Copy

Serial No. 09/855,030 Docket No. 492322001000 the first FET and the second FET having gate widths of about 700 μ m or less and not being connected to a shunt FET;

wherein the compound semiconductor devices are configured within the mobile communication device for switching between the signal receiving circuit and the signal transmitting circuit.

- 8. (Original) A mobile communication device according to claim 7, further comprising a second antenna, an antenna switch comprising one of said compound semiconductor switching devices for changing between the antenna and the second antenna for better reception or transmission of the signal, a filter switch comprising one of said compound semiconductor switching devices for changing between a filter for receiving the signal or for transmitting the signal and a band switch comprising one of said compound semiconductor switching devices for changing an IF band for receiving the signal or for transmitting the signal.
- 9. (Original) A mobile communication device according to claim 7, further comprising specialized circuitry for a mobile telephone, a Bluetooth device or a wireless LAN.
- 10. (New) A compound semiconductor switching device according to claim 1, wherein the common input terminal is configured to receive an input signal between about 2.4 GHz and about 3.0 GHz.
- 11. (New) A compound semiconductor switching device according to claim 1, wherein the gate widths of the first FET and the second FET are greater than or equal to 300 μ m.